claims, i.e., claims 21-23, 27-29, 33-35 and 39-41 have been amended to specify that the (at least) two chip electrodes are formed in a common wiring layer of the semiconductor chip.

No new matter has been entered. Pursuant to 37 CFR § 1.121, a marked copy of the amended claims showing changes made therein accompanies this Amendment.

Turning to the rejection of claims 21, 24, 27, 30, 33, 36, 39, 42, 45, 48, 51 and 54 under 35 U.S.C. 103(a) as being obvious over Applicant's admitted prior art in view of Rostoker (US Patent No. 5,399,898), Yoshizaki (US Patent No. 5,475,236) and Liang (US Patent No. 5,952,726), independent claims 21, 27, 33 and 39 all now specify that the "two chip electrodes are formed in a common wiring layer of said semiconductor chip." Applicant's admitted prior art teaches one electrode formed in the wiring layer. Applicant's admitted art does not teach two electrodes formed in a common wiring layer of a semiconductor chip. Further, Rostoker does not teach this feature. Rostoker teaches bump contacts disposed on the bottom surface of a substrate material 226 (col. 11, lines 35-38). Rostoker does not teach electrodes that are formed within a common wiring layer of a semiconductor chip. Yoshizaki also does not teach this feature. Yoshizaki teaches the common wiring 204 being separated from the electrodes 201 through a contact hole 203a. Yoshizaki does not teach at least two chip electrodes in a common wiring layer of the semiconductor chip. Finally, Liang teaches a method of arranging bump pads used to mount a flip-chip semiconductor die onto a substrate (col. 3, lines 60-65). Liang does not teach a chip electrode mounted within the wiring layer of a semiconductor chip. Furthermore, Liang is concerned with the distribution of solder bumps on the semiconductor die for mounting the die to a substrate (col. 3, lines 60-65; Figures 1 and 2; col. 4, lines 1-24). Liang does not teach arranging chip electrodes in a common wiring layer of

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the semiconductor from the edge of the chip towards its inner side or parallel edge of the chip. Thus, no combination of the applied art can achieve or render obvious the instant claims or any claims dependent therefrom.

Turning to the rejection of claims 22, 25, 28, 31, 34, 37, 40, 46, 49, 52 and 55 under 35 U.S.C. 103 as being obvious over the Applicant's admitted prior art in view of Rostoker, Yoshizaki, Liang and in further view of Fulcher (US Patent No. 5,686,764), claims 22, 34 and 40 have been amended to incorporate the limitations found in claims 21, 27, 33 and 39. Rostoker, Yoshizaki and Liang do not teach an electrode formed within a wiring layer of a semiconductor chip as discussed above. Fulcher also fails to teach this feature of claims 22, 28, 34 and 40. Fulcher teaches a bump pattern on the face of a die 10 to contact integrated circuits 12 (col. 3, lines 1-7; Figure 1). Fulcher does not teach two electrodes buried within a common wiring layer of the semiconductor chip. Thus, no combination of Applicant's admitted prior art, Rostoker, Yoshizaki, Liang and Fulcher could achieve or render obvious the instant claims or any claims dependent therefrom.

Turning to the rejection of claims 23, 26, 29, 32, 35, 38, 41, 44, 47, 50, 53 and 56 under 35 U.S.C. 103(a) as being unpatentable over the admitted prior art in view of Rostoker, Yoshizaki, Liang and in further view of Fulcher and Bertolet et al. (US Patent No. 5,844,317), these claims are patentable over Applicant's admitted art in view of Rostoker, Yoshizaki, Liang and Fulcher for the same reasons discussed above. Bertolet et al. teaches a wire bonding pad of the die beneath the conductive strap 16 (col. 7, lines 30-35; Figure 1). Bertolet et al. does not teach an electrode formed within a common wiring layer of a semiconductor chip. Therefore, no

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combination of the applied art could achieve or render obvious the instant claims or any claims dependent therefrom.

Having dealt with all the objections raised by the Examiner, the Application is believed to be in order for allowance.

The foregoing Amendment raises no new issues which require further search or consideration by the Examiner. Accordingly, entry of the foregoing Amendment and allowance of the Application are respectfully requested.

In the event there are any fee deficiencies or additional fees are payable, please charge them (or credit any overpayment) to our Deposit Account Number 08-1391.

Respectfully submitted,

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CERTIFICATE OF MAILING

I certify that this correspondence is being deposited with the United States Postal Service as First Class mail in an envelope addressed to "Assistant Commissioner for Patents, Washington, D.C. 20231" on March 10, 2003 at Tucson, Arizona.

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MARKED CLAIMS SHOWING CHANGES MADE

21. (Thrice Amended) A semiconductor device comprising:

a wiring substrate having a predetermined pattern of wiring formed on one surface;

a semiconductor chip disposed on the other surface of said wiring substrate and having at least one chip electrode set comprising at least two chip electrodes in a common wiring layer of said semiconductor chip, wherein said chip electrodes are arranged from an edge of said semiconductor chip toward its inner side;

said wiring substrate having a number of through-holes;

a number of bumps formed respectively in said through-holes of said wiring substrate in conforming relationship with said at least two chip electrodes and electrically connecting said wiring of said wiring substrate with said at least two chip electrodes; and

[a single] an external bump pad for said bump electrically connected [through said common wiring layer] to said at least two chip electrodes.

22. (Thrice Amended) A semiconductor device comprising:

a wiring substrate having a predetermined pattern of wiring formed on one surface;

a semiconductor chip disposed on the other surface of said wiring substrate and having at least one chip electrode set comprising at least two chip electrodes in a common wiring layer of said semiconductor chip, wherein said chip electrodes are arranged parallel to an edge of said semiconductor chip and said wiring is bent at at least one position;

said wiring substrate having a number of through-holes;

a number of bumps formed respectively in said through-holes of said wiring substrate in conforming relationship with said at least two chip electrodes and electrically connecting said wiring of said wiring substrate with said at least two chip electrodes; and

[a single] an external bump pad electrically connected [through said common wiring layer] to said at least two chip electrodes.

23. (Thrice Amended) A semiconductor device comprising:

a wiring substrate having a predetermined pattern of wiring formed on one surface;

a semiconductor chip disposed on the other surface of said wiring substrate and having at least one chip electrode set comprising at least two chip electrodes in a common wiring layer of said semiconductor chip, wherein said chip electrodes are arranged parallel to an edge of said semiconductor chip and said wiring has an end width larger than an inter-electrode distance between said chip electrodes;

said wiring substrate having a number of through-holes;

a number of bumps formed respectively in said through-holes in conforming relationship with said at least two chip electrodes and electrically connecting said wiring of said wiring substrate with said at least two chip electrodes; and

[a single] an external bump pad electrically connected [through said common wiring layer] to said at least two chip electrodes.

27. (Thrice Amended) A semiconductor device comprising:

a wiring substrate having a predetermined pattern of wiring formed on one surface;

a semiconductor chip disposed on said one surface of said wiring substrate and having at least one chip electrode set comprising at least two chip electrodes in a common wiring

layer of said semiconductor chip, wherein said chip electrodes are arranged from an edge of said semiconductor chip toward its inner side;

a number of bumps disposed on said wiring of said wiring substrate respectively in conforming relationship with said at least two chip electrodes and electrically connecting said wiring with said at least two chip electrodes; and

[a single] an external bump pad electrically connected [through said common wiring layer] to said at least two chip electrodes.

28. (Thrice Amended) A semiconductor device comprising:

a wiring substrate having a predetermined pattern of working formed on one surface;

a semiconductor chip disposed on said one surface of said wiring substrate and having at least one chip electrode set comprising at least two chip electrodes in a common wiring layer of said wiring substrate, wherein said chip electrodes are arranged parallel to an edge of said semiconductor chip and said wiring is bent at at least one position;

a number of bumps disposed on said wiring respectively in conforming relationship with said at least two chip electrodes and electrically connecting said wiring of said wiring substrate with said at least two chip electrodes; and

[a single] an external bump pad electrically [through said common wiring layer] to said at least two chip electrodes.

29. (Thrice Amended) A semiconductor device comprising:

a wiring substrate having a predetermined pattern of wiring formed on one surface;

a semiconductor chip disposed on said one surface of said wiring substrate and having at least one chip electrode set comprising at least two chip electrodes in a common wiring

layer of said semiconductor chip, wherein said chip electrodes are arranged parallel to an edge of said semiconductor chip and said wiring has an end width larger than an inter-electrode distance between said chip electrodes;

a number of bumps disposed on said wiring respectively in conforming relationship with said at least two chip electrodes and electrically connecting said wiring of said wiring substrate with said at least two chip electrodes; and

[a single] an external bump pad electrically connected [through said common wiring layer] to said at least two chip electrodes.

33. (Thrice Amended) A semiconductor device comprising:

a TAB (tape automated bonding) tape having a predetermined pattern of wiring formed on one surface;

a semiconductor chip disposed on the other surface of said TAB tape and having at least one chip electrode set comprising at least two chip electrodes in a common wiring layer of said semiconductor chip, wherein said chip electrodes are arranged from an edge of said semiconductor chip toward its inner side;

said TAB tape having a number of through-holes;

a number of bumps formed respectively in said through-holes in conforming relationship with said at least two chip electrodes and electrically connecting said wiring of said TAB tape with said at least two chip electrodes; and

[a single] an external bump pad electrically connected [through said common wiring layer] to said at least two chip electrodes.

34. (Thrice Amended) A semiconductor device comprising:

a TAB (tape automated bonding) tape having a predetermined pattern of wiring formed on one surface;

a semiconductor chip disposed on the other surface of said TAB tape and having at least one chip electrode set comprising at least two chip electrodes in a common wiring layer of said semiconductor chip, wherein said chip electrodes are arranged parallel to an edge of said semiconductor chip and said wiring of said TAB tape is bent at at least one position;

said TAB tape having a number of through-holes;

a number of bumps formed respectively in said through-holes in conforming relationship with said at least two chip electrodes and electrically connecting said wiring of said TAB tape with said at least two chip electrodes; and

[a single] an external bump pad electrically connected [through said common wiring layer] to said at least two chip electrodes.

35. (Thrice Amended) A semiconductor device comprising:

a TAB (tape automated bonding) tape having a predetermined pattern of wiring formed on one surface;

a semiconductor chip disposed on the other surface of said TAB tape and having at least one chip electrode set comprising at least two chip electrodes in a common wiring layer of said semiconductor chip, wherein said chip electrodes are arranged parallel to an edge of said semiconductor chip and said wiring of said TAB tape has an end width larger than an inter-electrode distance between said chip electrodes;

said TAB tape having a number of through-holes;

a number of bumps formed respectively in said through-holes in conforming relationship with said at least two chip electrodes and electrically connecting said wiring of said TAB tape with said at least two chip electrodes; and

[a single] an external bump pad electrically connected [through said common wiring layer] to said at least two chip electrodes.

39. (Thrice Amended) A semiconductor device comprising:

a TAB tape having a predetermined pattern of wiring formed on one surface;

a semiconductor chip disposed on said one surface of said TAB tape and having at least one chip electrode set comprising at least two chip electrodes in a common wiring layer of said semiconductor chip, wherein said chip electrodes are arranged from an edge of said semiconductor chip toward its inner side;

a number of bumps disposed on said wiring of said TAB tape respectively in conforming relationship with said at least two chip electrodes and electrically connecting said wiring of said TAB tape with said at least two chip electrodes; and

[a single] an external bump pad electrically connected [through said common wiring layer] to said at least two chip electrodes.

40. (Thrice Amended) A semiconductor device comprising:

a TAB tape having a predetermined pattern of wiring formed on one surface;

a semiconductor chip disposed on said one surface of said TAB tape and having at least one chip electrode set comprising at least two chip electrodes in a common wiring layer, wherein said chip electrodes are arranged parallel to an edge of said semiconductor chip and said wiring is bent at at least one position;

a number of bumps disposed on said wiring of said TAB tape respectively in conforming relationship with said at least two chip electrodes and electrically connecting said wiring of said TAB tape with said at least two chip electrodes; and

[a single] an external bump pad electrically connected [through said common wiring layer] to said at least two chip electrodes.

41. (Thrice Amended) A semiconductor device comprising:

a TAB tape having a predetermined pattern of wiring formed on one surface;

a semiconductor chip disposed on said one surface of said TAB tape and having at least one chip electrode set comprising at least two chip electrodes in a common wiring layer of said semiconductor chip, wherein said chip electrodes are arranged parallel to an edge of said semiconductor chip and said wiring has an end width larger than an inter-electrode distance between said chip electrodes;

a number of bumps disposed on said wiring of said TAB tape respectively in conforming relationship with said at least two chip electrodes and electrically connecting said wiring of said TAB tape with said at least two chip electrodes; and

[a single] an external bump pad electrically connected [through said common wiring layer] to said at least two chip electrodes.